

## REMARKS

In response to the above-identified Office Action, Applicant amends the application and seeks reconsideration thereof. Claims 12-14 are pending. The Examiner rejects Claims 12-14. Applicant amends Claims 12-14 and submits additional Claims 15-17 for consideration. Applicant contends that additional Claims 15-17 are fully disclosed in the specification and that no additional matter has been added therein.

Attached hereto is a marked-up version of the changes made to the specification and Claims by the current amendment. The caption is captioned "VERSION WITH MARKINGS TO SHOW CHANGES MADE."

### **I. In the Specification**

Applicants have amended the title in accordance with Examiner's request.

### **II. Claims Rejected Under 35 U.S.C. § 102**

The Examiner rejects Claims 12-14 under 35 U.S.C. 102(e) as being anticipated by Obeng et al ("Obeng"), U.S. Patent No. 6,323,131. The Patent Office states:

Regarding claim 12, Obeng et al. teaches an integrated circuit (Fig. 1(d)) comprising:  
a substrate having a circuit device;  
a dielectric material (10) over the circuit device with a via to the circuit device;  
a barrier material (18) lining the walls of the via;  
a seed layer overlying the barrier material and lining the walls of the via (Col. 4, lines 21-24); and  
a conducting material (20) directly contacting the circuit device.

Applicant respectfully disagrees and submits that Claims 12-14 are allowable for at least the reason that the prior art does not teach, suggest or describe a conductive material directly contacting a circuit device.

Independent Claim 12 includes "a conductive material directly contacting the surface of the circuit device." The Patent Office relied upon conductive material (20) in Obeng to address this feature. It is axiomatic that to be anticipated, every element of Claim 12 must be disclosed within a single reference. However, the Patent Office has not identified and applicant has been unable to find any teaching or suggestion in

Obeng that copper layer (20) directly contacts a circuit device. The portion of Obeng cited by the Patent Office describes integrating the use of self-assembled organic films into existing process steps for forming copper interconnections on ULSI circuits. For example, at col. 3, line 60 - col. 4, line 11, in relevant part, Obeng states:

The formation of copper interconnect layers on ULSI circuits and the passivation of the copper surfaces.... The Damascene process to generate an inlaid copper interconnection pattern and the CMP process are well known in the art and can be employed herein. These processes, as well as other well known prior art processes for depositing and patterning copper films for IC devices are referenced in and described by... which articles are incorporated herein by reference. Illustratively, use of the self assembled organic films can be integrated into existing processing steps as hereinafter described.

Moreover, Obeng then describes depositing a copper seed layer over a layer of the organic film (18) followed by capping the seed layer with a thick copper film (20), without removal of either the film (18) or copper seed layer. Thus, the organic film (18) and the seed layer are left between the added thick copper film (20) and the underlying substrate or components. For instance, as cited by the Patent Office, at col. 4, lines 21-24, Obeng describes:

A thin diffusion barrier/adhesion promoter film 18 may the be deposited, which again may be a self assembling organic film, followed by the deposition of a copper seed layer which is then capped with a thick copper film 20 by known techniques to give rise to the structure shown in FIG. 1(b).

Here, the via (16) is lined with barrier film (18) as well as copper seed in accordance with typical methods known in the art. Notably, as quoted above, this section of Obeng is directed to formation of the structure shown in Figure 1(b) of Obeng, which clearly shows diffusion barrier/adhesion promoter film 18 as well as a dark line layer (which although unlabeled in the figure, Applicant asserts is probably intended to represent the copper seed layer) between the thick copper film (20) and underlying silicon substrate (12)

In fact, most notably, Obeng actually claims a barrier layer under the copper interconnects. For example, Claim 8 of Obeng claims:

8. The integrated circuit set forth in claim 5 further comprising a barrier layer underlying said copper interconnects, said barrier layer consisting essentially of a self-assembled organic film.

This claim requires that a barrier layer underlie the copper interconnects and, therefore, exist between the copper interconnects and any substrate or circuit device underlying the interconnects. Hence, Applicant asserts that the point of Obeng is to form copper interconnects by using steps known typically in the art combined with using an organic film (i.e. using a chemistry not known typically in the art) for sealant film (14), thin diffusion barrier/adhesion promoter film (18), and/or spontaneous self-assembling film (24). However, Obeng does not describe a conductive material directly contacting a circuit device.

On the other hand, Applicant's Claim 12 includes "a conductive material directly contacting the circuit device." Thus, according to Claim 12, for example, a barrier material lining a via overlying a circuit device may have its surface coated with a seed layer such that relative to an etch process, the seed layer is substantially thicker on the walls of the via as opposed to the bottom or base of the via. The barrier layer at the bottom or base of the via can then be selectively etched because the barrier layer is substantially exposed at the bottom, while the barrier layer at the walls is substantially coated by the seed layer, thus, prohibiting etching of the barrier layer at the walls. As a result, the barrier layer can be removed (e.g. by etching) from the bottom or base of the via to expose the underlying circuit device so that subsequent deposition of a conductive material can form a direct contact between the conductive material and the underlying circuit device. On the other hand, as explained above, Obeng describes the forming of copper interconnects in steps known typically in the art, including by forming a barrier layer and a seed layer in the bottom of the via and leaving those layers in the bottom of the via during deposition of thick copper film (20). Thus, as shown in Figure 1(b), Obeng describes a barrier layer and a seed layer remaining in the via, in between the thick copper film (20) and underlying silicon substrate (12). Therefore, the conductive material in direct contact with the circuit device of Applicant's Claim 12 is distinct from the copper layer (20) having a barrier film (18) and a copper seed layer between it and substrate (12), of Obeng. Applicant respectfully requests that the Patent Office withdraws the rejection of Claim 12 under 35 U.S.C. § 102(e).

**III. Dependent Claims 13-14.**

Applicant respectfully submits that Claims 13-14 being dependent upon respective allowable base Claim 12 are also not anticipated by Obeng, for at least the foregoing reasons. Applicant respectfully requests that the Patent Office withdraw the rejection of Claim 13-14 under 35 U.S.C. § 102(e).

**CONCLUSION**

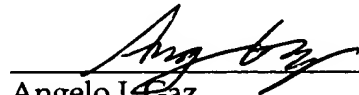
In view of the foregoing, it is believed that all claims now pending (1) are in proper form, (2) are neither obvious nor anticipated by the relied upon art of record, and (3) are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

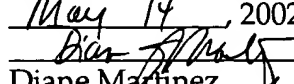
Dated: 5/14/02, 2002

  
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**CERTIFICATE OF MAILING:**

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Box Non-Fee Amendment, Assistant Commissioner for Patents, Washington, D.C. 20231, on

May 14, 2002.  
  
Diane Martinez [Date]

Attachment: Version With Markings to Show Changes Made

"VERSION WITH MARKINGS TO SHOW CHANGES MADE"

IN THE SPECIFICATION

The title has been amended as follows:

**~~A PROCESS TO MANUFACTURE CONTINUOUS METAL~~  
INTERCONNECTS**

IN THE CLAIMS

The claims have been amended as follows:

12. (Amended) An integrated circuit comprising:

a substrate having a circuit device;

a dielectric material overlying the circuit device with a via formed in the dielectric material to the circuit device, the via exposing a sidewall in the dielectric material and a surface of the circuit device;

a barrier material substantially lining the sidewall~~a wall or walls~~ of the via;

a seed layer ~~onoverlying~~ the barrier material and substantially lining the sidewall~~wall or walls~~ of the via; and

a conductive material directly contacting the surface of the circuit device.

13. (Amended) The integrated circuit of claim 12~~10~~, wherein the circuit device comprises~~is~~ an interconnection line.

14. (Amended) The integrated circuit of claim 12~~10~~, wherein the conductive material is copper.

Claims 15-17 have been added:

15. (New) The integrated circuit of claim 12, wherein the barrier layer comprises an etch characteristic such that the barrier material can be selectively etched in the presence of the seed material.

16. (New) An integrated circuit comprising:

a substrate having a circuit device;

a dielectric material overlying the circuit device with a via formed in the dielectric material to the circuit device, the via exposing a sidewall in the dielectric material and a surface of the circuit device;

a barrier material substantially lining the sidewall;

a seed layer on the barrier material and substantially lining the sidewall; and

a conductive material in the via;

wherein the seed layer and barrier material are formed so as to expose the circuit device at an end of the via

17. (New) The integrated circuit of claim 16, wherein the barrier layer comprises an etch characteristic such that the barrier material can be selectively etched in the presence of the seed material.